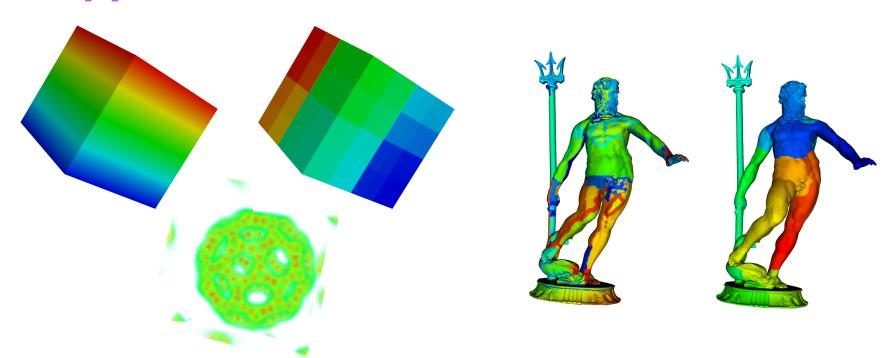
Cache-Oblivious Algorithms Application to Scientific Visualization



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CEA/DAM/DIF







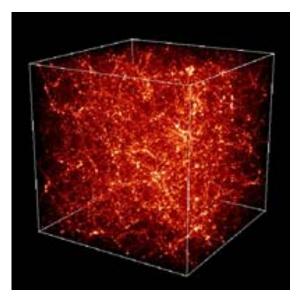




Visualization & Massive Data Sets



TERA-10
CEA supercomputer
19th Top500
9968 Itanium2
60 Tflops
30 TB of memory
1 PB of disk space



Simulation of half the observable universe 50 TB mesh

How do we visualize massive data sets?

Techniques to Handle Massive Data Sets

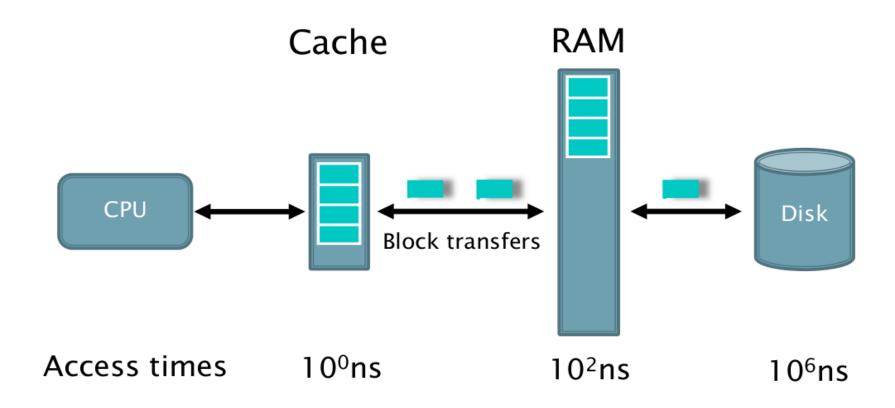
- Data Compression
 - Geometry compression
 - Topology compression
 - Attributes compression
- Cache-conscious techniques — Today's topic
 - Data reordering
 - Computation reordering

Outline

« An algorithm is said **oblivious** if no program variables dependent on hardware configuration parameters need to be tune to reach optimal performances » [Prokop&al]

- Cache-Aware Model
- Cache-Oblivious Model
- Cache-Oblivious Mesh Layout
- Preliminary Experiments
- Conclusion & Future Work

Memory Hierarchy



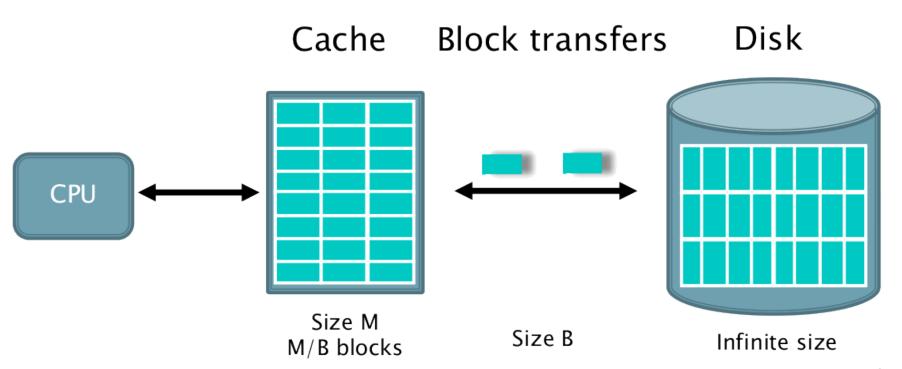
Cache-Aware Model (CA)

[Aggarwal & Vitter 1988]

or external memory out-of-core disk access machine I/O model

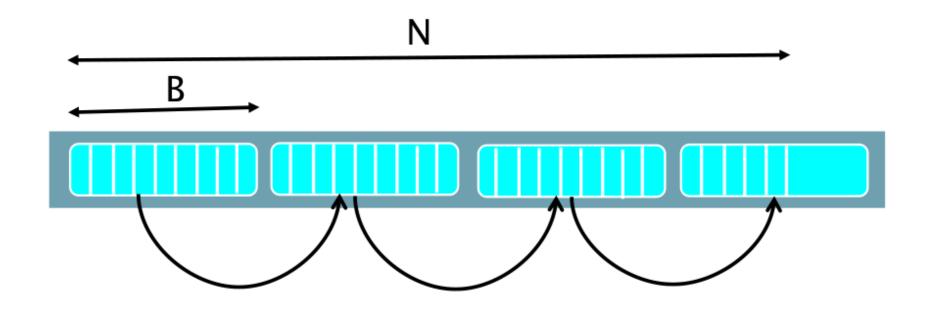
W: #operations

Q: #block transfers



Scanning in the CA Model

Read an N-elements array: the naive algorithm is optimal

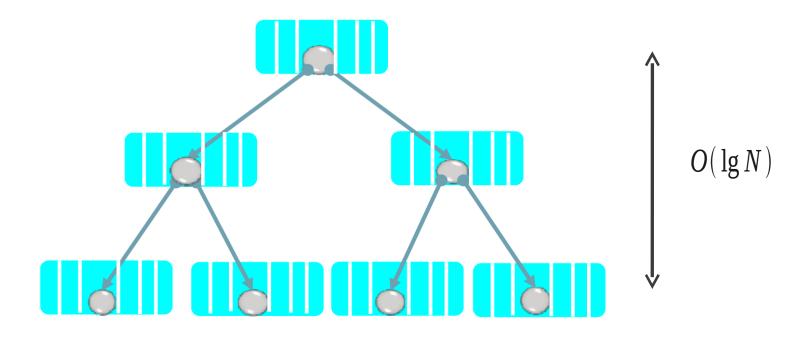


$$W(N)=N$$

$$Q_{CA}(N)=\lceil N/B \rceil$$

Searching in the CA Model

Searching a key in an N-nodes balanced binary tree: naive doesn't work



$$W(N)=1.O(\lg N)$$

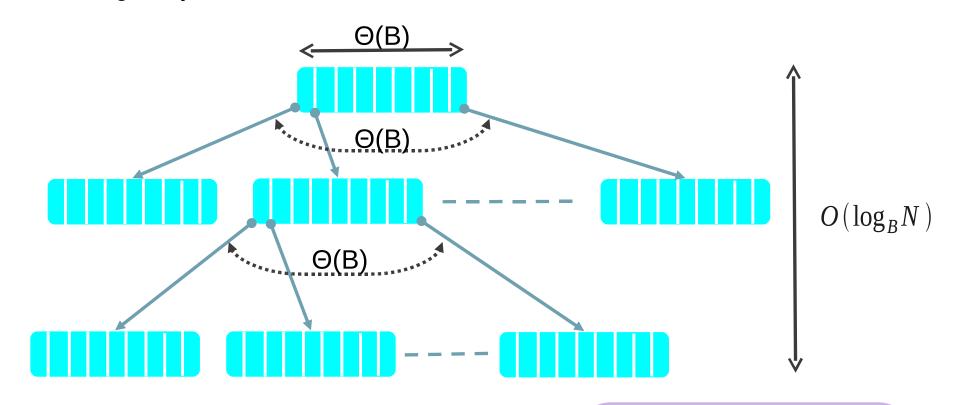
 $Q_{naive}(N)=1.O(\lg N)$

$$W(N)=O(\lg N)$$

 $Q_{naive}(N)=O(\lg N)$

Searching in the CA Model

Searching a key in an N-elements B-tree



$$W(N) = \lg B.O(\log_B N)$$

$$Q_{CA}(N) = 1.O(\log_B N)$$

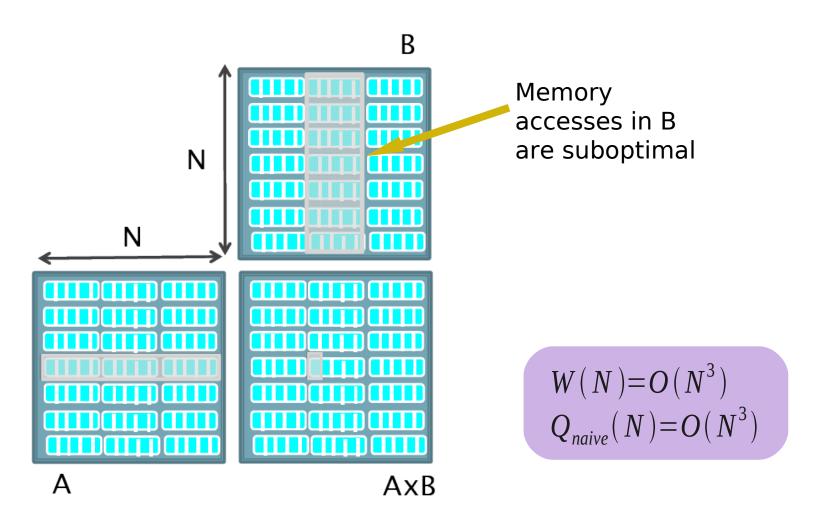
$$W(N)=O(\lg N)$$

$$Q_{naive}(N)=O(\lg N)$$

$$Q_{CA}(N)=O(\log_B N)_9$$

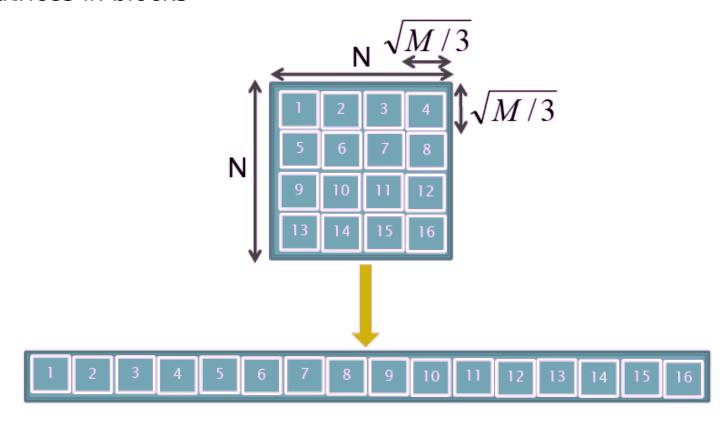
Multiplying in the CA Model

NxN matrices in row-major order: naive doesn't work



Multiplying in the CA Model

NxN matrices in blocks



Technique used in BLAS

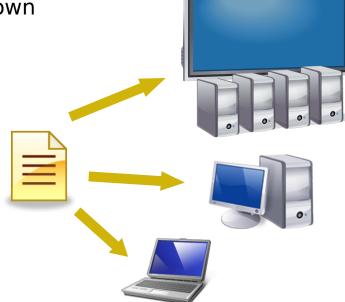
$$Q_{naive}(N) = O(N^{3})$$

$$Q_{CA}(N) = O\left(\frac{N^{3}}{B\sqrt{M}}\right)$$

Drawbacks of the CA Model

- Only two levels of the memory hierarchy
 - At least 4 levels on any modern CPU
 - Even deeper with multiprocessors
- + Efficient with all levels of the memory hierarchy

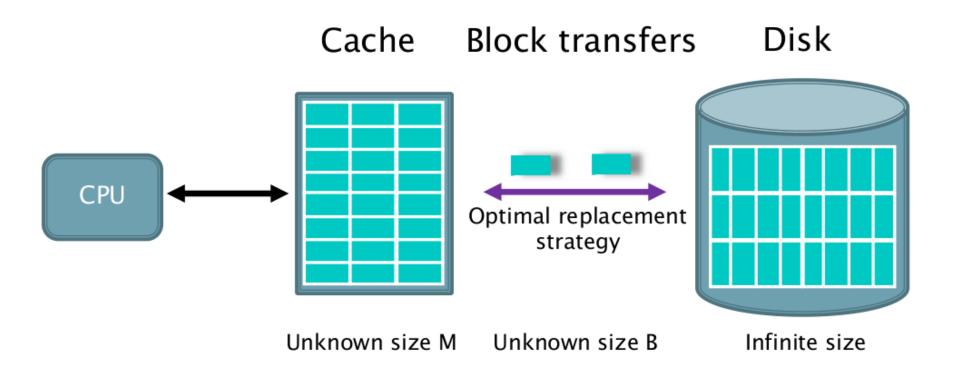
- Architecture dependent
 - Difficult to find optimal B and M (ATLAS)
 - GPU memory hierarchy is unknown
 - B and M can vary over time
 - Need to recompute the layout



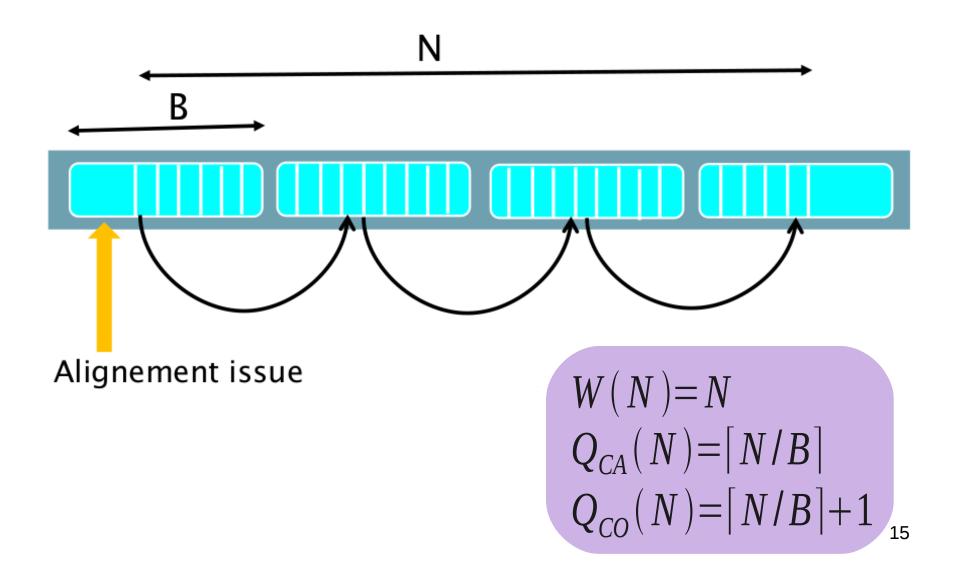
+ Architecture independent

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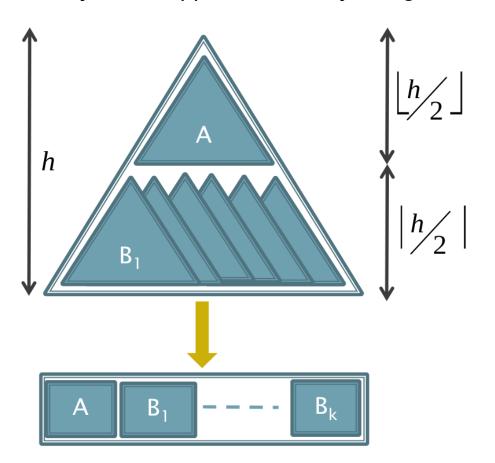
Scanning in the CO Model

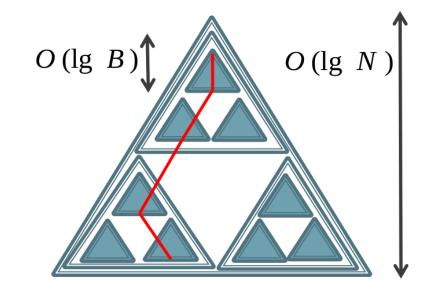


[Bender et al 2000]

Searching in the CO Model

Binary tree mapped in memory using a recursive layout



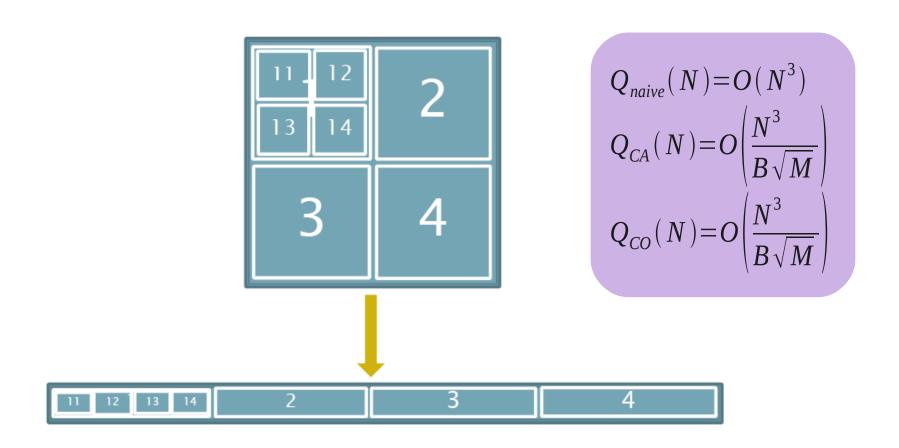


$$Q_{CO}(N) = O(1) \cdot \frac{O(\lg N)}{O(\lg B)}$$

$$Q_{CA}(N) = O(\log_B N)$$
$$Q_{CO}(N) = O(\log_B N)$$

Multiplying in the CO Model

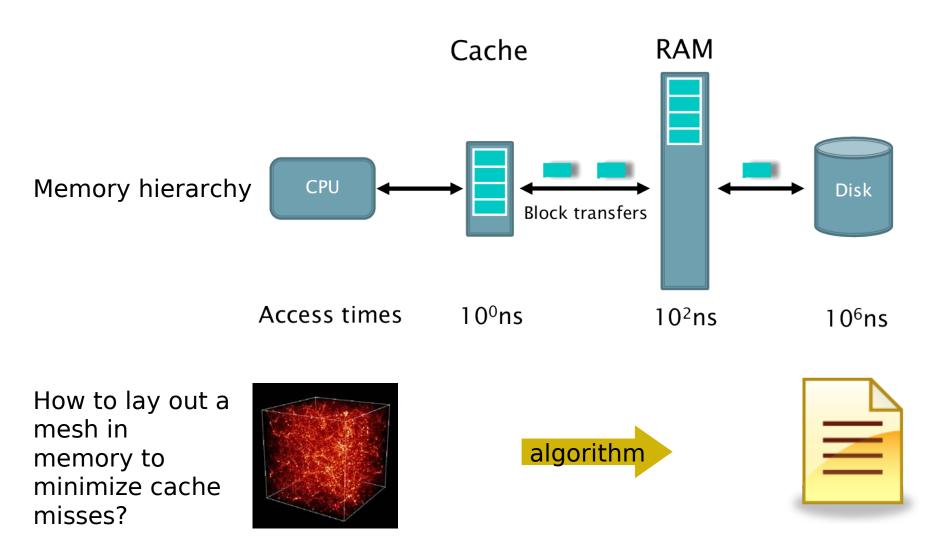
D&C matrix multiplication using a recursive layout



Outline

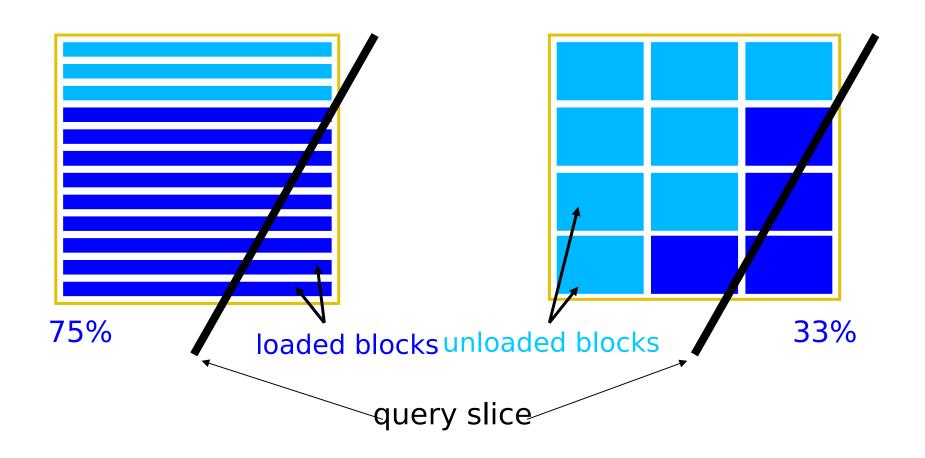
- Cache-Aware Model
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Cache-Oblivious Ordering of a Mesh

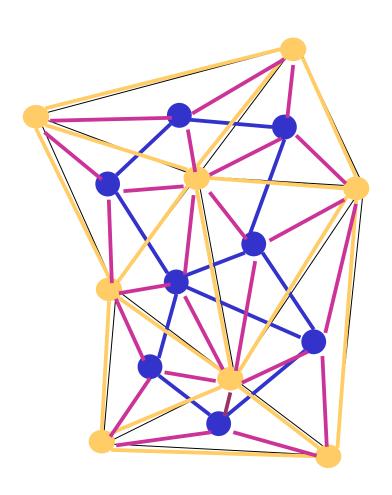


Idea

Triangles (or vertices) that are most likely to be accessed sequentially should be stored nearby



Graph of Sequential Accesses



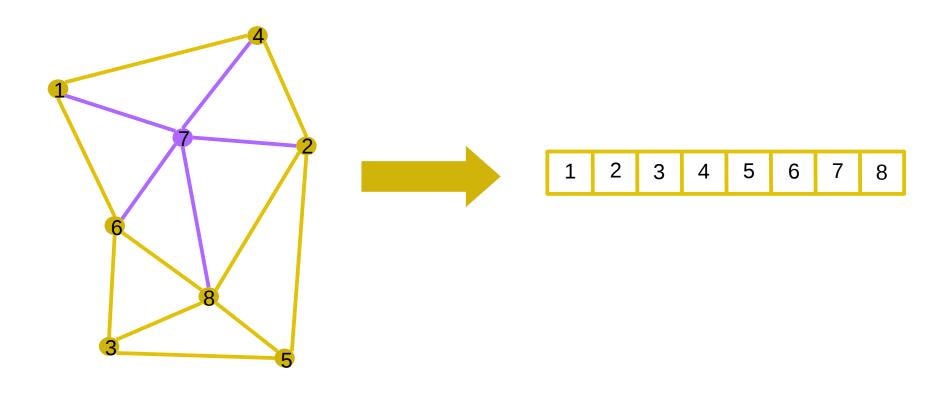
G₁: sequential access between triangles

G₂: sequential access between vertices

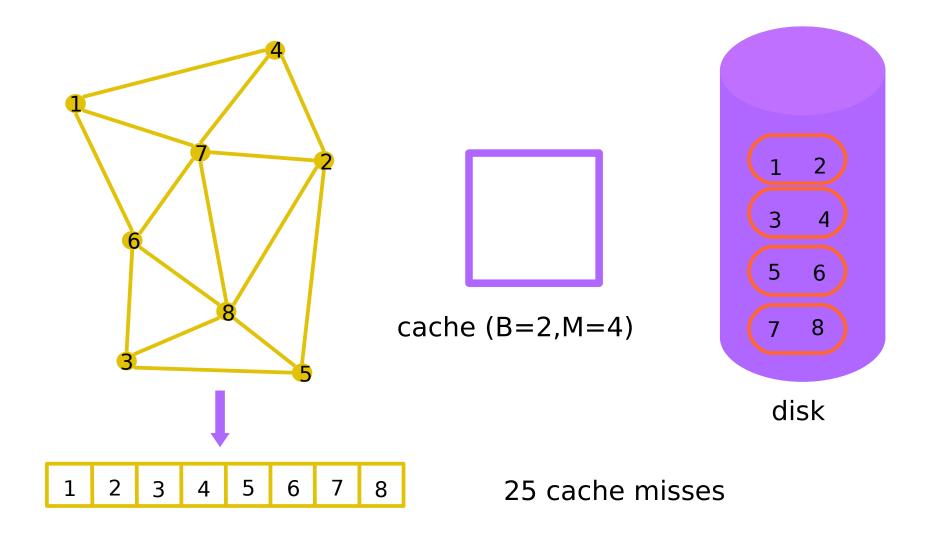
G₃: both

Mesh Layout Problem

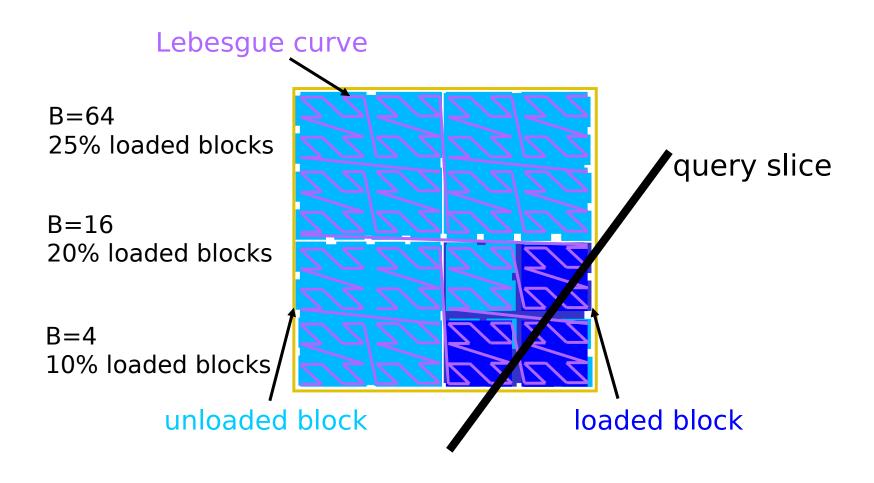
Minimize # of cache misses if each node touches all its neighbors



Example

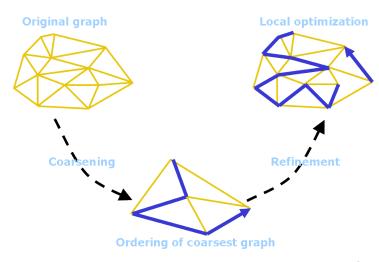


Regular Meshes: Space-Filling Curves



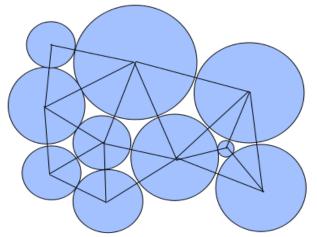
Unstructured Meshes

- Heuristic algorithm based on multi-level optimization
 - slow
 - high memory usage
- Good experimental results (2-5x improvement)
- But no guarantee on
 - time to compute the layout
 - layout quality



Overlap graphs

- Planar graphs
 - Egde between two nodes iff two circles touch each other
- Overlap graphs (extension in dimension d)
 - Edge between two nodes iff two spheres touch each other
- Overlap graphs contain well-shaped meshes

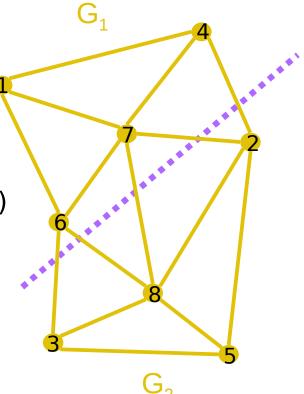


Separate the mesh into two roughly equal-size pieces cutting few edges

• |
$$G_1$$
|, | G_2 | $\leq \frac{1}{3}$ | G | | $E(G_1, G_2) \leq \sqrt{8|G|}$

• Overlap graphs (randomized linear time) $|G_1|, |G_2| \leq \frac{2raphs}{d+2}|G|$

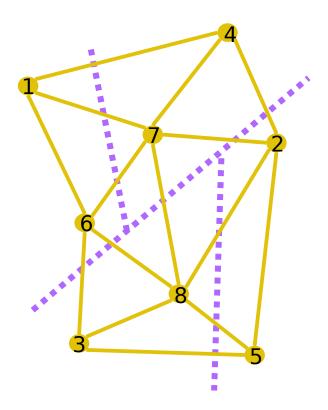
$$E(G_1, G_2) = O(|G|^{1-1/d})$$

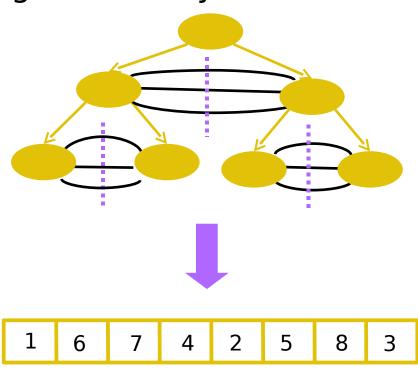


Our layout

$$W(N) = O(N \log N)$$

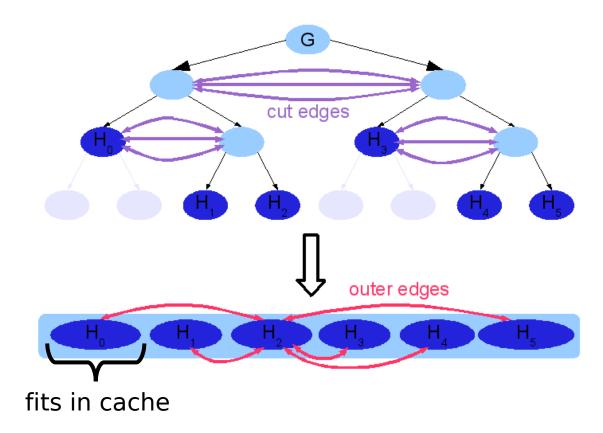
- Recursively cut the mesh
- The order of the leaves gives the layout





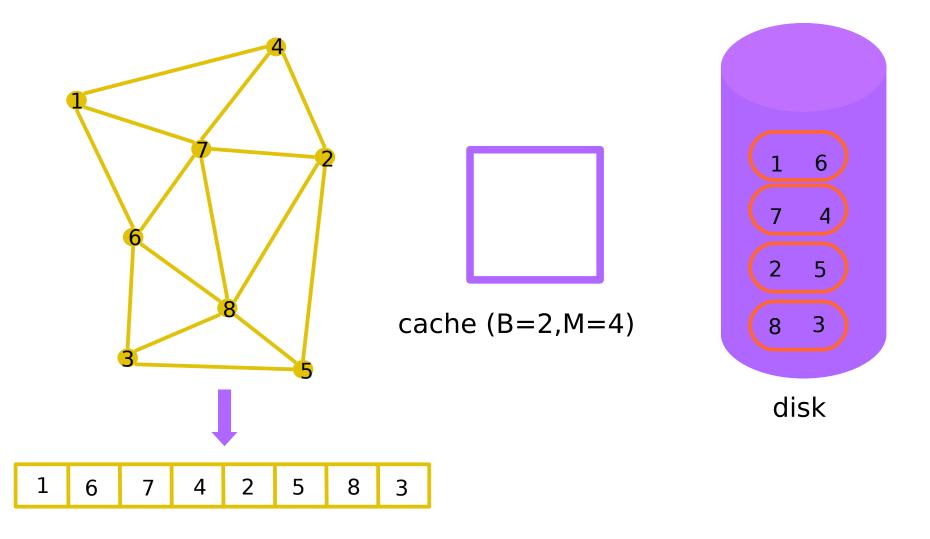
Guarantee on the Quality of the Layout

- Each subgraph fits in cache
- Edges inside a subgraph do not cause a cache miss
- Cache misses are bounded by the number of edges between two subgraphs (outer edges)
- One can show that there are few outer edges



Theorem: Our layout guarantees that a traversal of an O(N)-size d-dim mesh causes less than $O(N/B+N/M^{1/d})$ cache misses

Back to the Example

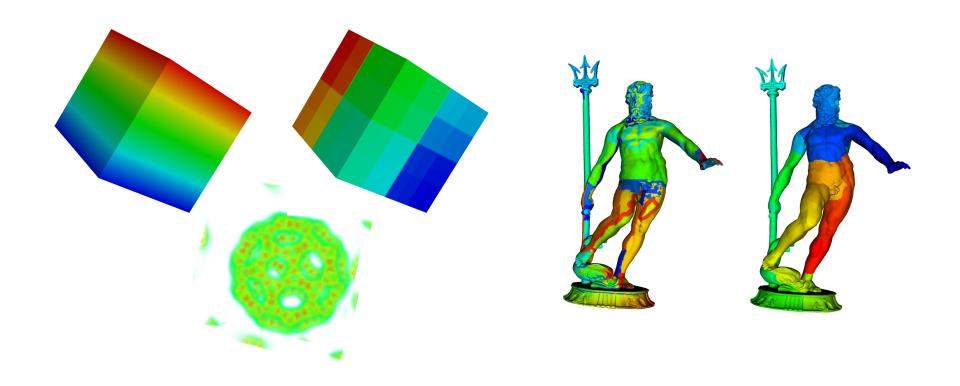


12 cache misses (25 previously)

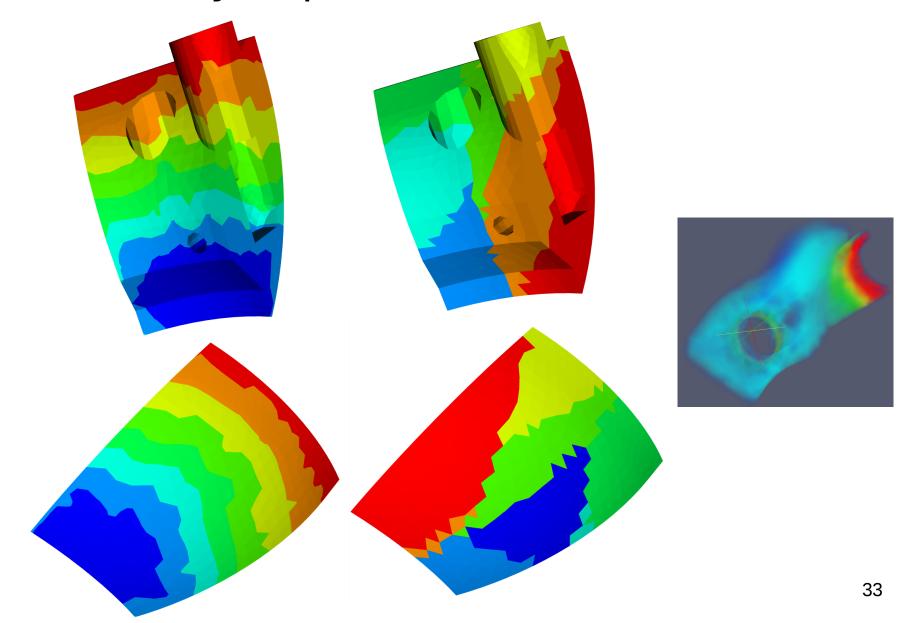
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Preliminary Experiments

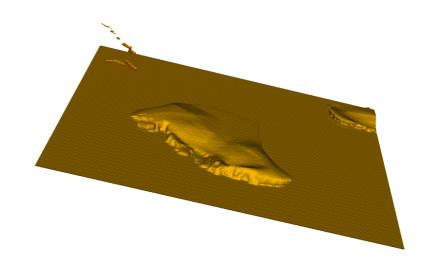


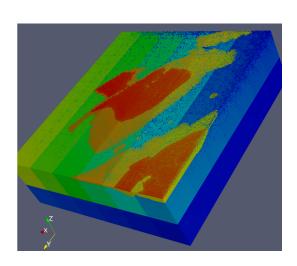
Preliminary Experiments

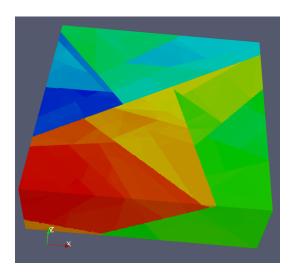


Isosurface extraction

- Marching Cube (On CPU with VTK)
- Marching Cube (On GPU with CUDA)
- Using a tree to speed up cell search
 - Tree from VTK
 - Our tree (min-max tree)



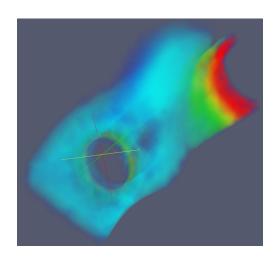


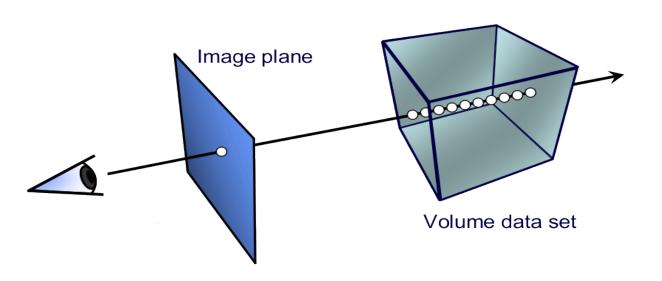


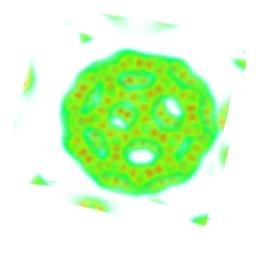
2,4M points 14M tetras

Volume Rendering

- Using VTK on CPU (several methods)
- Our code in CUDA on GPU







Outline

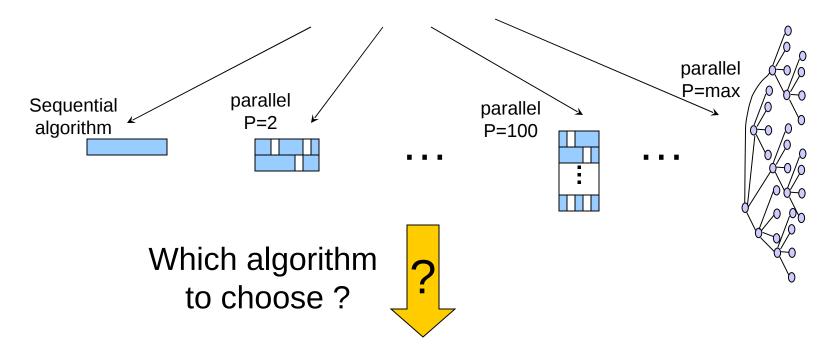
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Conclusion & Future Work

- Our algorithm
 - Fast
 - Quality & time guarantee
 - Architecture independent
- Experimental validation
 - Difficult to find big 3D unstructured meshes
 - Multiresolution methods
- Visualization in parallel
 - How do we keep the good cache performance ?

Processor oblivious algorithms

To design a single efficient algorithm with provable performances on an arbitrary architecture













A processor & cache oblivious model

Deeper memory hierarchy

```
SMT/HT (L1)

Multicore (L2/L3)

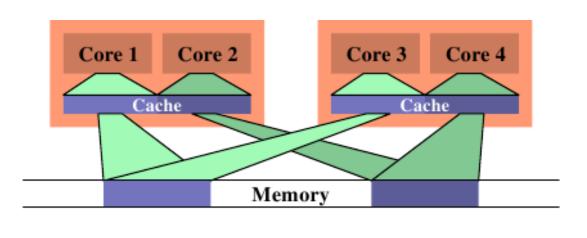
NUMA/SMP (RAM)

Cluster (Small network)

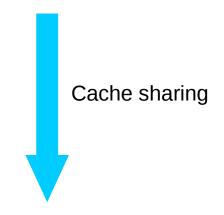
Grid (Large Network)
```

- Processor + Cache → Communications
 - sharing a cache ↔ low cost communication

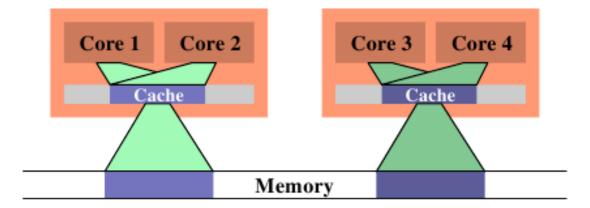
Interaction cache / scheduling



Can be worse than each core has a cache of half size



Can be as good as each core has a cache of full size



Questions?

Thank you